XPERT SOLVER
ORDER NOW Submit

Decoders and Encoders

Objectives:

The objective of the lab is to study the operation of Encoders and Decoders using QUARTUS II.

Apparatus:

QUARTUS II (Altera Corp.).
ALTERA University DE2-115 board with Cyclone IV EP4C115F29C7 FPGA
74138 Octal Decoder
7447 BCD to Seven Segment Decoder
74147 Encoder
Seven Segment display

Discussion:

Decoder is a logical device which takes a binary input from a user and selects one of the output corresponding to that binary. Each binary combination represents a certain output. This mean that for **'n'** inputs, there will be **'2^n'** outputs.

An encoder work on the opposite principle to the decoder, encoder accepts a single input and converts the input into the consecutive output binary. This means that for every **'2^n'** inputs, there are **'n'** output binary combinations. Encoders and decoders are used in many logical circuits like BCD seven segment delays. The information send to SSD is encoded by the encoder which represents that which of the leds need to be on or off.

Procedure:

Operation of 74138 – One of Eight Decoder

1. Created a new project with the name **'decoder'**.
2. Created a graphic file named **'decoder.bdf'** and drew the structure of decoder (shown below).
3. Inputs were labeled **A,B,C and Enable** while outputs were labeled **Y0, Y1, … , Y7.**
4. Selected **Project ➔ Top List Entity** and compiled the project.

XpertSolver.com

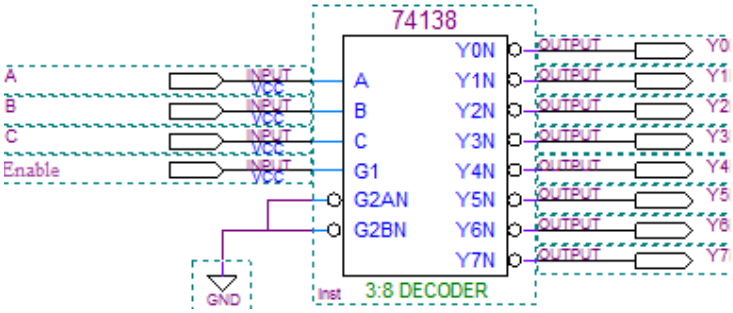

Figure 1 Decoder Circuit Structure

5. Created a waveform file named **decoder.vwf** and input waveform was defined as shown below.
6. **Simulator Mode** was set to functional from the pull down menu.
7. The created input file was used and **Functional Netlist** was generated.
8. Project was simulated and outputs were recorded.

Results:

1. The output waveform came out to be:

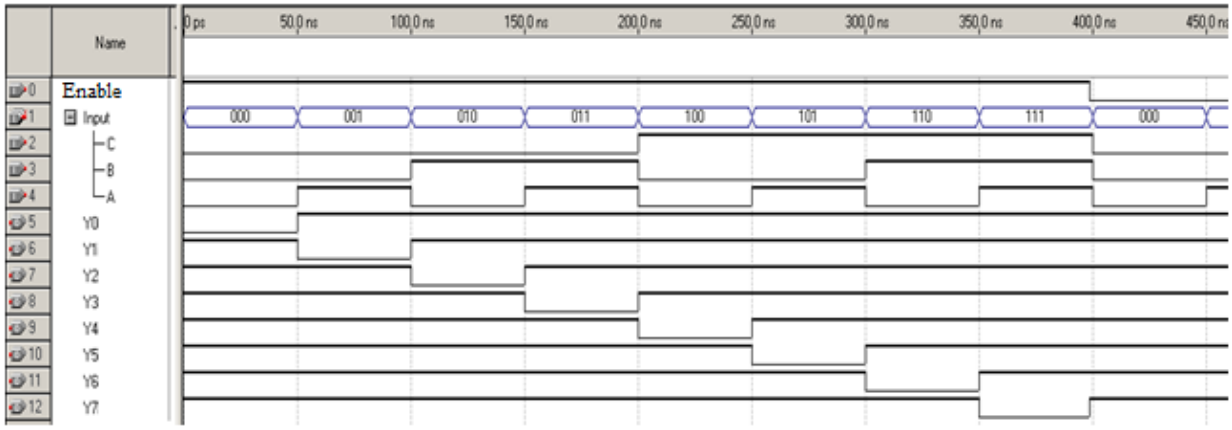

Figure 2 Input waveforms for Decoder

2. The following values of A,B and C are required too enable Y6.
   A = _____ B = _____ C = _____
3. In case of **LOW Enable** , the output values will be :
   _____-
4. The tow output _____ be enabled simultaneously because _____
5. The output values corresponding to A, B, C = 101 are:
   _____------

6. The outputs are recorded as shown below:

Enable	C	B	A	Time Interval	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
				000- 050 ns								
				050-100 ns								
				100-150 ns								
				150-200 ns								
				200-250 ns								
				250-300 ns								
				300-350 ns								
				350-400 ns								
				400-450 ns								
				450-500 ns								
				500-550 ns								
				550-600 ns								
				600-650 ns								
				650-700 ns								
				700-750 ns								

Operation of 74147 – Decimal to BCD Encoder

1. Created a new project with the name **'encoder'** and generated and schematic named **'encoder.bdf'**.
2. The schematic drawn is show below. Inputs namely **1-9** and outputs **a, b, c, d, e, f and g** were labeled.

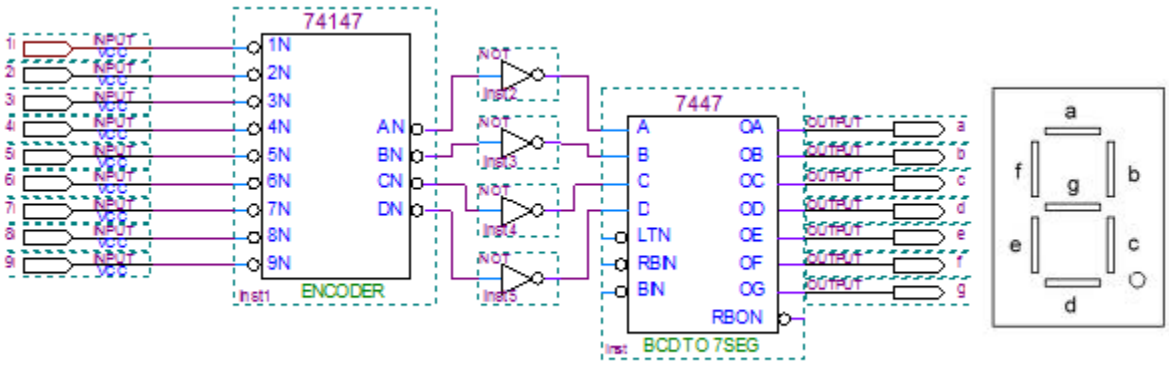

Figure 3 SSD Encoder interfaced with FPGA Structire

3. Selected **Project ➔ Top Level Entity.**
4. Compiled the project:
5. Programmed the FPGA to show the output generated from BCD to the SSD available on the FPGA. Pin assignments were studied and followed.

XpertSolver.com

6. Recompiled the project and downloaded the project o-board:
    a. Connected DE2 board to usb port and powered it.
    b. Selected **Tools | Prorammer**.
    c. Locate and add the **'encoder.pof'** file.
    d. Download the program.
7. Tested the program by keeping all the toggle switches initially to **HIGH** and giving one low input every time. Outputs were observed.

Results

1. If the inputs **4** and **8** were active low at the same time, the result was:

_____

2. The outputs obtained by toggling different switches are tabulated below:

1	2	3	4	5	6	7	8	9	Display
1	1	1	1	1	1	1	1	1	
0	1	1	1	1	1	1	1	1	
1	0	1	1	1	1	1	1	1	
1	1	0	1	1	1	1	1	1	
1	1	1	0	1	1	1	1	1	
1	1	1	1	0	1	1	1	1	
1	1	1	1	1	0	1	1	1	
1	1	1	1	1	1	0	1	1	
1	1	1	1	1	1	1	0	1	
1	1	1	1	1	1	1	1	0	

Figure 4 SSD Outputs for different encoder values.

Appendix

Input/Output	Switch/LED	PIN
1	SW8	PIN_AC25
2	SW7	PIN_AB26
3	SW6	PIN_AD26
4	SW5	PIN AC26
5	SW4	PIN AB27
6	SW3	PIN AD27
7	SW2	PIN AC27
8	SW1	PIN AC28
9	SW0	PIN AB28
Output	**Signal**	**PIN**
a	HEX0[0]	PIN_G18
b	HEX0[1]	PIN_F22
c	HEX0[2]	PIN_E17
d	HEX0[3]	PIN_L26
e	HEX0[4]	PIN_L25
f	HEX0[5]	PIN_J22
g	HEX0[6]	PIN_H22

Figure 5 Pin Configuration